

I claim:

1. An integrated memory, comprising:

bit lines;

word lines intersecting said bit lines at points of intersection;

memory cells disposed at said points of intersection between said word lines and said bit lines;

at least one reference word line intersecting said bit lines at points of intersection;

reference cells disposed at said points of intersection between said at least one reference word line and said bit lines, said reference cells generate a reference potential on said bit lines before an access operation to one of said memory cells;

a redundant word line intersecting said bits lines at points of intersection;

redundant memory cells disposed at said points of intersection between said redundant word line and said bit lines; and

[illegible]

said programmable activation unit has a first subunit and a second subunit connected to said first subunit, said first subunit is used to distinguish if said redundant word line replaces one of said word lines or said reference word line during the operation of the integrated memory, said second subunit determines an instant at which said redundant word line is activated by said programmable activation unit during the access operation to one of said memory cells;

if one of said word lines is being replaced by said redundant word line, said second subunit does not activate said

[illegible]